International Journal of Electrical and Electronics Engineering Research (IJEEER)
ISSN(P): 2250-155X; ISSN(E): 2278-943X
Vol. 4, Issue 1, Feb 2014, 23-34

TRANS STELLAR
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CLOSED LOOP CONTROL OF ZVS, ZCS INTERLEAVED BOOST - CONVERTER WITH PID CONTROLLER

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ABSTRACT

An enhanced soft switching technique for an interleaved boost converter has better performance characteristics when compared to conventional boost converter. As IBC operates under soft switching the main devices do not have any additional voltage & current stress on the auxiliary devices are at low level. Where main switches operates out of phase and share the output current while providing soft switching condition for each other IBC with ZCS&ZVS during ON&OFF conditions of the main switches, that can drive large load operated in duty cycle greater than 50% & less than 50% is proposed in this study. In this paper an improved switching technique for an closed loop interleaved boost converter with PID controller and open loop interleaved boost converter is proposed. IBC which effectively reduces the ripple current in input current & output voltages as function of duty cycle. Which also increase in efficiency, greater reliability and also increase in stability of the system due to closed loop control and comparison between the IBC with PID and IBC and conventional boost converter had done for various duty cycles.

KEYWORDS: Interleaved Boost Converter, Soft Switching, ZVS, ZCS, Ripple, PID Controller, Reliability, Efficiency, Stability

INTRODUCTION

The boost converter is a popular choice for most power electronics systems to serve as a pre- regulator, due to advantages of simplicity & high performance. Interleaving technique meritoriously increases the switching frequency without increasing the switching losses, thereby increase in the power density without compromising efficiency. Interleaving reduces the output capacitor ripple current as a function of duty cycle. To reach the smooth soft switching, the circuits consist of auxiliary circuits which totally decrease the conduction loss by achieving the zero voltage switching and zero current switching condition. A better soft switching circuit is proposed, but the converter works in discontinuous mode with duty cycle less than and greater than 50%, auxiliary. The higher switching frequency may cause the higher switching losses, higher electro- magnetic interference (EMI) and the lower overall efficiency.

This paper proposes a novel interleaved boost converter with both characteristics of zero-voltage turn-ON and zero-current turn-OFF for the main switches to improve the efficiency with a wide range of load. The voltage stresses of the main switches and auxiliary switch are equal to the output voltage. The proposed converter is the parallel of two boost converters and their driving signals stagger 180° and this makes the operation assumed symmetrical. Moreover, by establishing the common soft-switching module, the soft-switching interleaved converter can further reduce the size and cost.

DESIGN AND ANALYSIS

Figure 1 shows the proposed circuit. It uses the interleaved boost topology and applies the common soft-switching circuit. The resonant circuit consists of the resonant inductor L_r, resonant capacitor C_r, parasitic capacitors C_{Sa} and C_{Sb}, and auxiliary switch S_r to become a resonant way to reach ZVS and ZCS functions.

Operational Analysis of D < 50% Mode

The operating principle of the proposed topology is described in this section. There are 24 operational modes in the complete cycle. Only the 12 modes related to the main switch S_a are analyzed, because the interleaved topology is symmetrical. Figure 3 shows the related wave forms when the duty cycle of the main switch is less than 50%.

The circuit is operated in fundamental mode with duty cycle D which is exact symmetrical in function. The circuit is analyzed with certain assumption to simplify the circuit analysis which is listed as:

- All power switches and diodes are ideal.
- The input inductor and output capacitor are ideal.
- The two inductors are equal; Boost_L_1= Boost_L_2
- The duty cycles of the main switches are equal;D_1=D_2

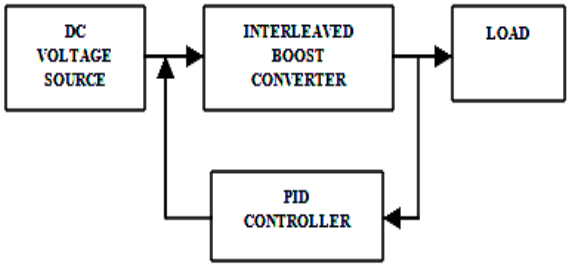


Figure 1: Block Diagram of Closed Loop Control of Interleaved Boost Converter

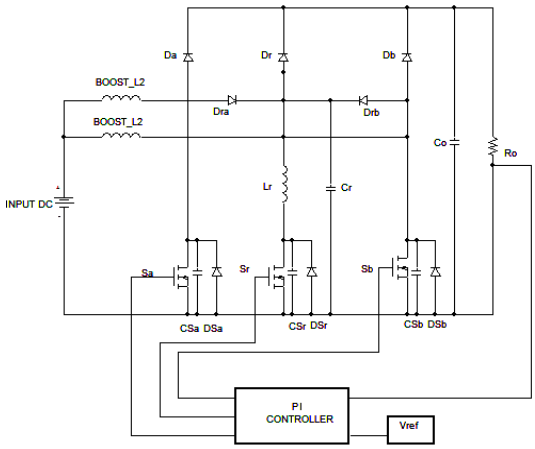


Figure 2: Circuit Diagram of Closed Loop Control of IBC with PID Controller

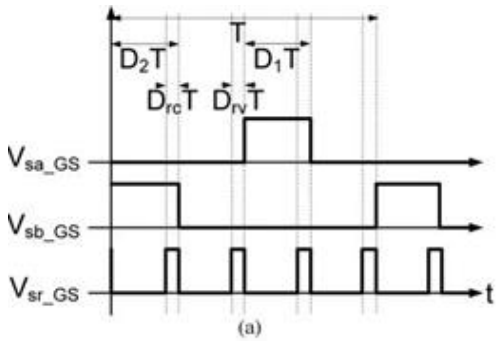


Figure 3: Switching Sequence of Main and Auxiliary Switches

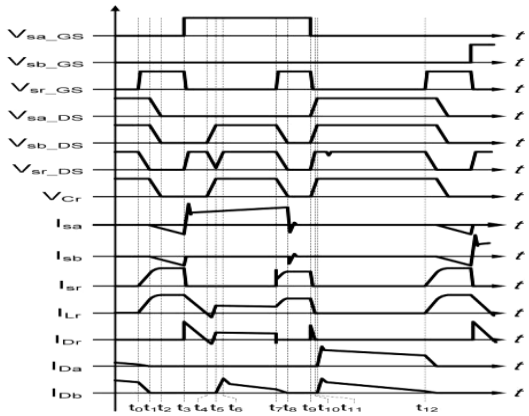


Figure 4: Related Wave Form of Proposed Converter for Duty Cycle D<50%

Mode1 [t_o-t_1]

Figure 5(a) shows equivalent circuit. In this mode, the main switches, S_a and S_b are turned OFF, the auxiliary switch S_r and the rectifier diodes D_a and D_b are turned ON, and the clamped diode Dr is turned OFF. The voltage across the parasitic capacitors C_{sa} and C_{sb} of the main switches and resonant capacitor Cr are equal to the output voltage i.e, $V_{sa}=V_{sb}=V_{sr}=V_o$.

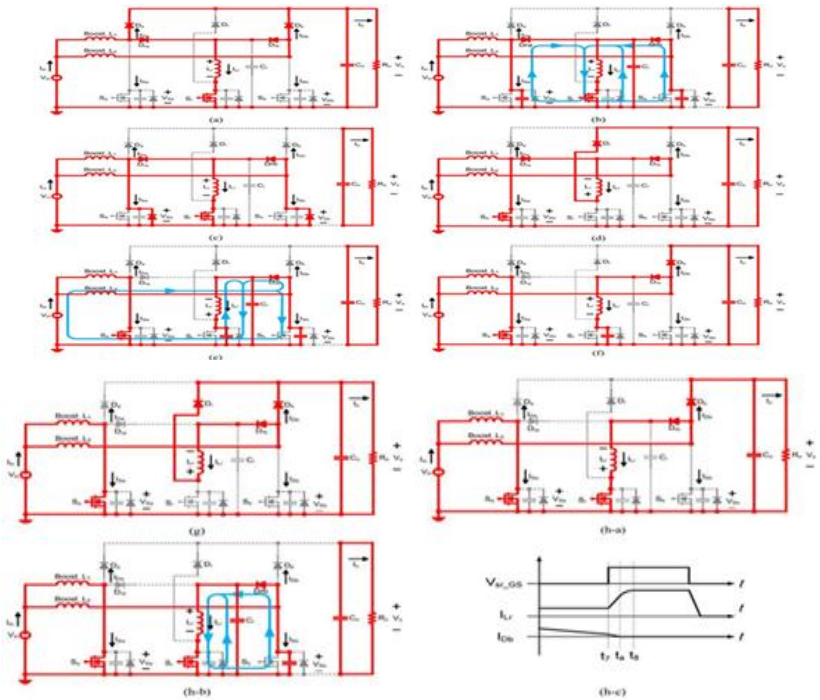
$$t_{01} = L_r \frac{I_{in}}{V_o} \tag{1}$$

Mode2[t_1-t_2]

In mode2 due to resonance action between jjj the parasitic capacitors C_{sa} C_{sb} C_r and L_r main switch voltages will reach to zero and body diodes D_{sa} D_{sb} will turn ON. Simultaneously resonant inductor current increased to reache the peak value.The resonant time t_{12} and inductor current I_{Lr} is given by

$$t_{12} = \frac{\pi}{2\omega_0} = \frac{\pi}{2}\sqrt{L_r\,(c_{sa} + C_{sb} + C_{sr})} \tag{2}$$

where $\omega_0 = \frac{1}{\sqrt{L_r\,(c_{sa}+C_{sb}+C_{sr})}}$,



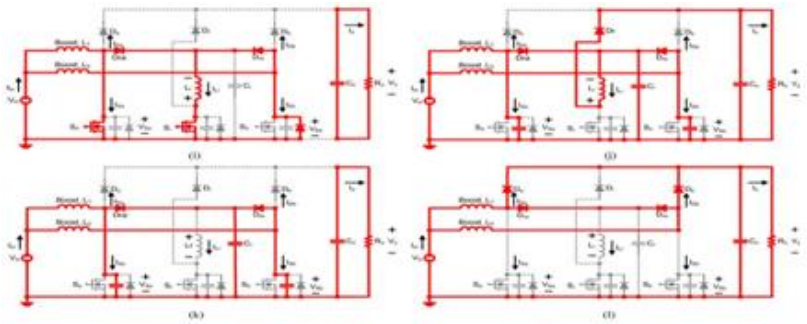


Figure 5: Equivalent Circuits of Different Modes (D<50%) (A) Mode 1[T0-T1] (B) Mode 2[T1-T2] (C) Mode 3[T2-T3] (D) Mode 4[T3-T4] (E)Mode 5[T5-T6] (F) Mode 6[T6-T7] (G) Mode7[T7-T8] (H)Mode 8[T8-T9](I)Mode 9[T9-T10](J)Mode10[T10-T11],(K)Mode 11[T11-T12],(L)Mode 12[T12-T13]

Mode 3 [t_2-t_3]

As in mode 2 the voltage across the main switches reaches to zero therefore at this time , main switch can achieve ZVS providing on-time of auxiliary switch S_r greater than the $t_{01}+t_{02.}$

The interval time t_{03} is.

$$t_{03} \geq t_{01}+t_{12}=L_r.\frac{I_{in}}{V_o}+\frac{\pi}{2}.\sqrt{L_r.(c_{sa}+C_{sb}+C_{sr})} \quad (3)$$

Mode 4 [t3-t4]

Figure (d) shows the equivalent circuit of this mode. In this mode the auxiliary switch Sr is turned OFF and the clamped diode D is turned ON. In this mode resonant inductor Lr is transferred to the output load. The energy discharge time of the resonant inductor is

$$t_{34}=\frac{L_r}{V_o}(I_{in}+\frac{V_o}{\sqrt{L_r/(c_{sa}+C_{sb}+C_{sr}}}) \quad (4)$$

Mode 5[t4-t5]

In this mode, the clamped diode Dr is turned OFF. the rectifier diode Db is turned ON when the voltage across the main switch Sb reachesVo. The resonant time is given by

$$t_{45}=\pi\sqrt{\frac{L_r C\ C_{sr}}{C+C_{sr}}} \quad (5)$$

where $C = Cr + CSb$

Mode 6[t5-t6]

The parasitic capacitor Csr, of the auxiliary switch is linearly charged by IL2-I0 to Vo. Then, the clamped diode Dr is turned ON. The interval time t56 is

$$t_{56}=\frac{C_{sr}.V_o}{I_{L2}-I_o} \quad (6)$$

Mode 7[t6-t7]

In this mode clamped diode Dr is turned ON. The energy stored in the resonant inductorLr is transferred to the out put load by the clamped diode Dr. end of the mode Dr is turned OFF due to auxiliary switch turned ON

$$t_{67}=D_1\text{T-}(D_{rc}\text{T}+t_{36}) \quad (7)$$

Mode 8[t7-t8]

As the current in inductor reaches to IL2 the diode current will be zero and attain off condition. The interval time is given by

$$t_{78}==L_r.\frac{I_0}{V_o}+\frac{\pi}{2}.\sqrt{L_r.(C_{sb}+C_{sr})} \quad (8)$$

Mode 9[t9-t10]

The main switch Sa attain the ZCS condition and turn off by reaching the inductor current greater than the Iin value. The interval time is given by

$$t_{89}=D_1\text{T-}t_{38} \quad (9)$$

Mode 10[t10-t11]

When the main switch Sa and auxiliary switch Sr are turned OFF, the energy stored in the resonant inductor Lr is transferred to the output load by the clamped diode Drb.

$$t_{9-10}=\frac{L_r}{V_o}\left(i_{L_r}(t_a)+\frac{V_o}{\sqrt{L_r/_{(C_r+C_{sb})}}}\right) \quad (10)$$

Mode 11[t10-t11]

The capacitors Csa, Csb and Cr are linearly charged by Iin to Vo and the rectifier diodes Da and Db are turned ON . the interval time is given by

$$\mathrm{t_{10-11}}=\frac{(\mathrm{c_{sa}+C_{sb}+C_r}).(\mathrm{V_o-V_{cr}(t_{10})})}{\mathrm{I_{in}}} \quad (11)$$

Mode 12[t11-t12]

The ending time t12 is equal to the operation of the interleaved topology is symmetrical. The interval time is given by

$$t_{11-12}=\frac{T}{2}\text{-}(D_1T+\ t_{03}+t_{9-11}) \quad (12)$$

Voltage Conversion Ratio for D<50% is given by

$$\frac{V_o}{V_{in}}=\frac{1}{1-(D_1+D_{rc}+2D_{rv})} \quad (13)$$

Operational Analysis of D>50% Mode

The principle of the proposed topology operated in D>50% mode is described in this section. There are 14 operational modes in the complete cycle. Only seven modes related to the main switch Sa analyzed. Because interleaved topology is symmetrical. Switching wave forms are given by

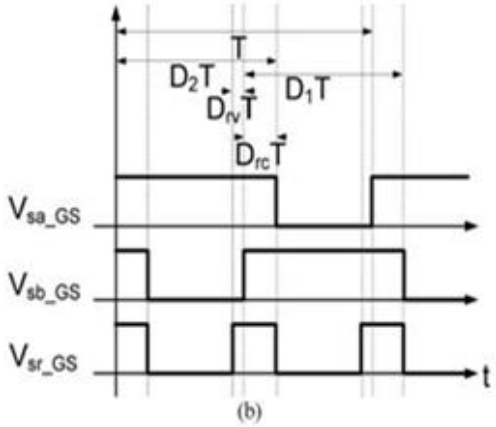


Figure 6: Switching Wave Forms of Main and Auxilary Switches

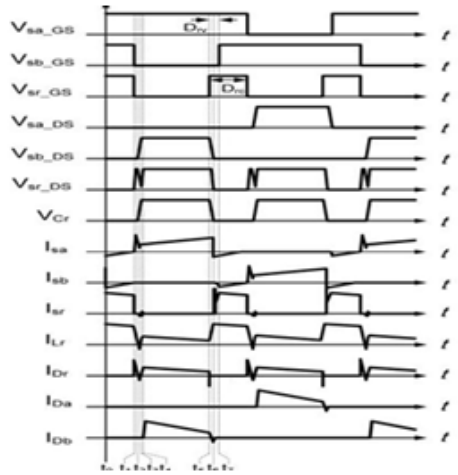


Figure 7: Switching Waves for D>50%

Mode1[t0-t1]

In this mode Sa Sb and Sr are turned ON, and the rectifier diodes Da and Db and clamped diode Dr are turned OFF. The main switch Sb can achieve the ZCS characteristic at end of the mode. The interval time is given by

$$t_{01}=(D_1 - t_{07})T \tag{14}$$

Mode2[t1-t2]

In this mode auxiliary switch Sr is turned OFF. When the resonant inductor current ILr decreases linearly until it reaches zero at end of the mode, the calmped diode Dr is truned OFF. The interval time is given as

$$t_{12}=\frac{L_r}{V_o} I_{in} \tag{15}$$

Mode3[t2-t3]

In this mode, the clamped diode Dr is turned OFF. The rectifier diode Db is turned ON when the main switch voltage Vsb and resonant capacitor voltage Vcr increase to Vo. The time interval is given by

$$t_{23}=\pi \sqrt{\frac{L_r C C_{sr}}{C+C_{sr}}} \tag{16}$$

Mode4[t3-t4]

The parasitic capacitor Csr of the auxiliary switch is linearly charged by IL2-Io to Vo. Then, the clamped diode Dr is turned ON at end of the mode. The interval time is given as

$$t_{34}=\frac{C_{sr}.V_o}{I_{L2}-I_o} \quad (17)$$

Mode5[t4-t5]

In this mode clamped diode is turned OFF due to energy stored in the inductor Lr is transferred to the output load by the clamped diode Dr. The interval time is given by

$$t_{45}=0.5T-t_{04}-D_{rv}T \quad (18)$$

Mode6[t5-t6]

In this mode the rectifier diode Db is turned OFF and the resonant inductor current continues to increase to the peak value and the main switch voltage Vsb decreases to zero because of the resonance among Csb,Cr and Lr. At end of the mode Ds+b is turned ON.

$$t_{56} = L_r \frac{I_o}{V_o} + \frac{\pi}{2}\sqrt{L_r(C_{sb} + C_r)} \quad (19)$$

Mode7[t6-t7]

In this mode main switch Sa can be turned OFF under the ZCS condition. Due to main switch current is less than or equal to zero.

$$t_{67}=0.5T-t_{06} \quad (20)$$

The Voltage Conversion Ratio for D>50% is given by

$$\frac{V_0}{V_{in}} = \frac{1}{1-(D_1+D_{rc})} \quad (21)$$

CONDITION OF SOFT SWITCHING

Condition of Zero Voltage Switching

To achieve the aim if the ZVS of the main switches +the voltage across Sa and Sb in mode2 for D<50% and Mode6 for D>50% must be assured to decrease to Zero.

For D<50%

$$D_{rv}T > t_{12} = \frac{\pi\sqrt{L_r(C_{sa}+C_{sb}+C_r)}}{2} \quad (22)$$

For D>50%

$$D_{rv}T > t_{56} = \frac{\pi\sqrt{L_r(C_{sb}+C_r)}}{2} \quad (23)$$

Condition of Zero Current Switching

For D<50%

$$t_{78}==L_r.\frac{I_0}{V_o}+\frac{\pi}{2}.\sqrt{L_r.(C_{sb}+C_r)} \quad (24)$$

For D>50%

$$t_{78}==L_r.\frac{I_0}{V_o}+\frac{\pi}{2}.\sqrt{L_r.(C_{sb}+C_r)} \quad (25)$$

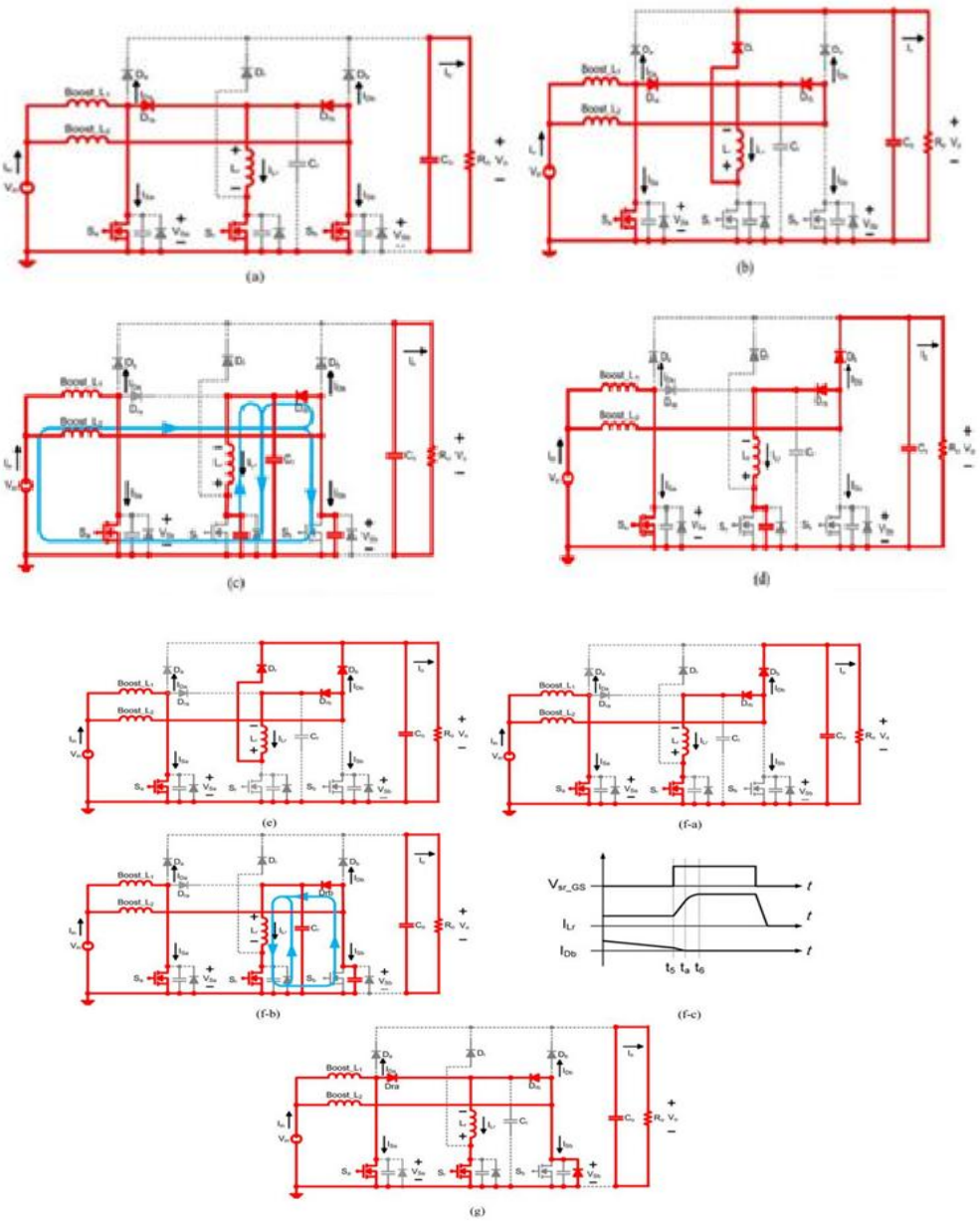


Figure 8: Equivalent Circuits of Different Modes(D>50%) (a) Mode1[t0-t1] (b) Mode2[t1-t2] (c)Mode3[t2-t3] (d) Mode4[t3-t4] (e) Mode5[t4-t5] (f) Mode 6[t5-t6] (g)Mode 7[t6-t7]

Table 1: Parameters and Components of the Converter

Input voltage	vo	150	250
Duty cycle	D	D<50%	D>50%
Output voltge	Vo	400V	
Output current	Io	0.5A~1.5A	
Output power	Po	200W~600W	
Switching frequency	Fs	50KHz	
Boost_L1,L2		2.4mH	
Output capacitor	co	470µF	
Resonant inductor	Lr	10µH	
Resonant ca pacitor	Cr	1.5nF	

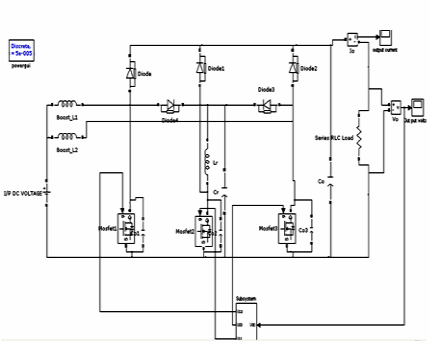


Figure 9: Simulation Circuit for Closed Loop Control of Interleaved Boost Converter with PID Controller

SIMULATION RESULTS

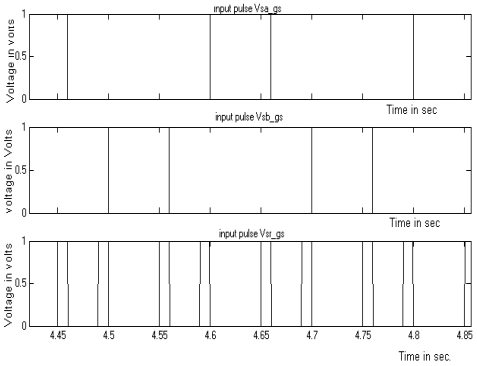


Figure 10: Switching Wave Forms of IBC for Duty Cycle D<50%

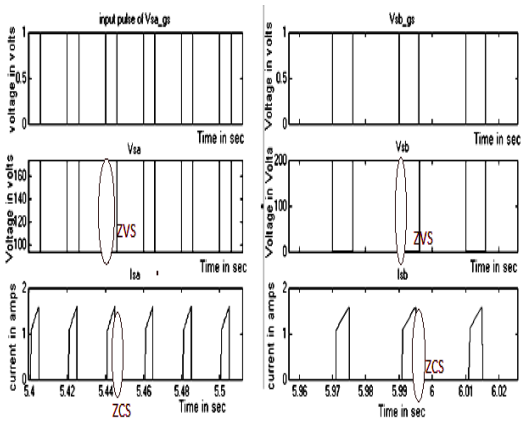


Figure 11: ZVS, ZCS Condition of IBC for D<50%

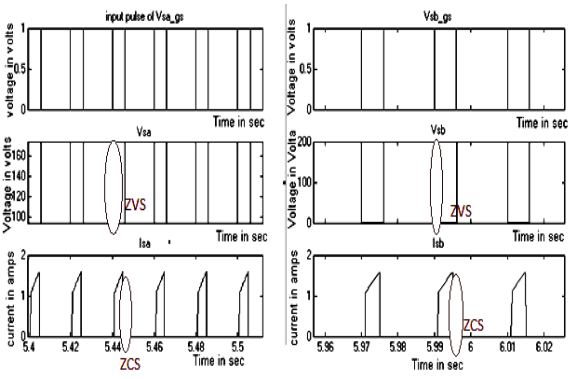


Figure 12: ZVS, ZCS Condition of IBC for D>50%

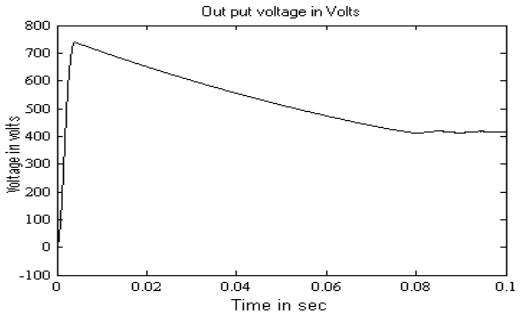


Figure 13: Output Voltage of IBC

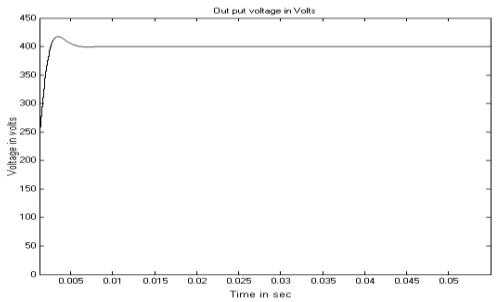


Figure 14: Output Voltage of IBC with PID

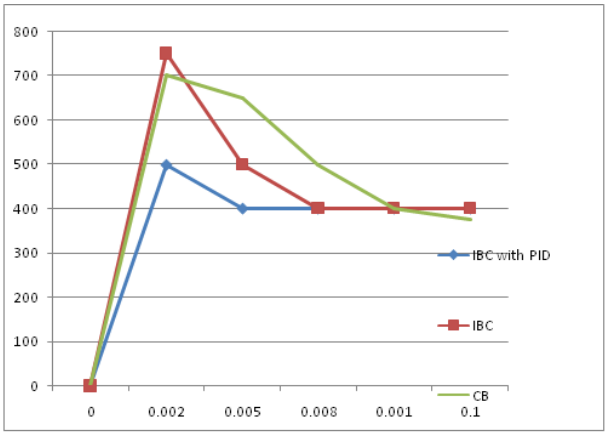


Figure 15: Measurement of Settling Time between IBC with PID, IBC, Conventional Boost Converter

Table 2: Comparison between IBC with PID and without PID & Conventional Boost Converter for D=30%

Sl No	Parameters	IBC without PID	IBC with PID	Conventional Boost Converter
1	Input voltage	250	250V	250V
2	Duty cycle	30%	30%	30%
3	Input current	2.92A	2.14A	1.918A
4	Output current	1.5A	1.5A	1.342A
5	Input current ripple	0.36A	0.41A	0.624A
6	Output voltage	400V	400V	357.14V
7	Output voltage ripple	0.013V	0.013V	0.017V
8	Settling time	0.08sec	0.005 sec	0.2Sec
9	efficiency	99.97	99.9%	98.8%

Table 3: Comparison between IBC with & without PID and CB for D<50% i.e, 15%

S. No	Parameters	IBC without PID	IBC with PID	Conventional Boost Converter
1	Input voltage	250V	250V	250V
2	Duty cycle	15%	15%	15%
3	Input current	2.2A	2.27A	1.3A
4	outputcurrent	1.25A	1.27A	1.105A
5	Input current ripple	0.14	0.01A	0.3125A
6	Output voltage	334.3V	334.3V	294.11V
7	Output voltage ripple	0.005A	0.003	0.007V
8	Settling time	0.08sec	0.05sec	0.1sec
9	efficiency	99.98	99.99	99.92%

Table 4: Comparison of IBC with and without PID for D>60%

S No	Parameters	IBC with Out PID	IBC with PID	Conventional Boost Converter
1	Input voltage	150V	150V	150V
2	Duty cycle	60%	60%	60%
3	Input current	5.98A	3.759A	3.524A
4	output current	1.5A	1.5A	1.409A
5	Input current ripple	0.28A	0.73A	0.75A
6	output voltage	400V	400V	375V
7	output voltage ripple	0.017V	0.017V	0.035V
8	Settling time	0.087sec	0.01sec	0.38Sec
9	efficiency	99.98	99.9%	98.8%

Table 5: Comparison between IBC with PID and without PID and CB for D>50% I.E, D=75%

S No	Parameters	IBC without PID	IBC with PID	Conventional Boost Converter
1	Input voltage	150V	150V	150V
2	Duty cycle	75%	75%	75%
3	Input current	28.09A	29.01A	9.02A
4	output current	03.01A	3.01A	2.25A
5	Input current ripple	0.7A	0.012A	0.93A
6	output voltage	765V	765V	600V
7	output voltage ripple	0.05V	0.002V	0.071V
8	Settling time	0.1sec	0.06sec	0.12sec
9	efficiency	99.97	99.9%	99.98

CONCLUSIONS

The above paper has discussed principle and operation of open loop interleaved boost converter and closed loop boost converter by using soft switching techniques. The features and performance of interleaved boost converter system under various duty cycles had been investigated. The accurance of ZVS and ZCS conditions and out put voltages of interleaved boost converter had been simulated using MATLAB & SIMULINK and different parameters are compared between conventional boost converter, interleaved boost converter with and with out PID controller by using soft switching techniques. There fore the ripple reduction , increase of stability, efficiency and switching losses can be greatly reduced.

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